In the Specification:

Please amend the fourth paragraph beginning on page 1, line 20 as follows:

--As is also known in the art, a DRAM chip typically includes two regions: memory array regions; and, non-memory array regions. These non-memory array regions are generally referred to as regions peripheral to the array regions or merely as peripheral regions. More particularly, referring to FIG. 1, a semiconductor wafer 10 is shown having a plurality of identical semiconductor chips 12. The fabricated chips 12 are then separated along the scribe lines 14. The borders of the scribe lines 14 are shown more clearly in FIG. 2 and are designated as 14a, 14b, such as FIG. 2 showing a portion of the wafer 10 shown in FIG. 1. Thus, an exemplary one of the chips 12 is shown in detail in FIG. 2 to include memory array regions, here four memory array regions 16 and peripheral regions 17. Each array region 16 includes the DRAM memory cells and associated row and column decoders, not shown. The peripheral regions 17 typically include decoders and sense amplifiers, not shown. Also included in the peripheral region 17 of each chip 12 is, in this example, a pair of voltage generators 20. Also disposed in the peripheral regions 17 are power busses 22 which electrically interconnect the voltage generators 20 to the array regions 16. In a conventional DRAM semiconductor chips, the voltage generators 20 occupy up to several percent of the total chip 12.--

Please amend the third paragraph beginning on page 6, line 22 as follows:

--Having fabricated the semiconductor wafer 30 as shown in FIGS. 3 and 4, a dielectric member 49, such as a thin printed circuit board, shown more clearly in FIG. 6 is provided with patterned ~~electrical~~ electrically isolated electrical conductors 52 on one surface, here the inner surface of the dielectric member 49. The dielectric member 49 has an electrical contact 55 on the

opposite, here outer surface thereof as indicated. The contact 55 is electrically connected to the electrical conductor 52 through via conductor 57. The dielectric member 49 may be a single member having the conductors formed on one surface of such member ~~50~~ 49, as shown in FIGS. ~~5 and 6~~ 5, 6 and 7. The dielectric member 49 may be a multi-level, e.g., laminated member, having electrical conductors 52 in various dielectric layers thereof. In either case, one inner surface of the dielectric member 49 has at least one electrical conductor 52 which is electrically connected to the electrical contact 55 using a conductive via 57. The dielectric member 49, here having a diameter the same, or larger than the diameter of wafer 30, is placed over the surface of the wafer 30 as indicated in FIG. 6, here the electrical conductors 52 are indicated by hatched lines for convenience.--

Please amend the first full paragraph on page 7 beginning at line 3 as follows:

--Thus, a dielectric member 49 is provided having electrical conductors 52. The dielectric member 49 is positioned over the wafer 30 with the electrical conductors 52 being ~~disposed on~~ located above the plurality of electrical contacts 53 and with such electrical conductors 52 spanning the separating regions 33, as indicated in FIGS. 5 and 6. It is noted then that the electrical conductor 52 ~~is thus~~ may be electrically connected to the buss 50 through the contacts 53, as noted above.--

Please amend the second full paragraph on page 7 beginning at line 9 as follows:

--Next, as illustrated in FIG. 7, the positioned dielectric member 49 is electrically connected to contacts 53 on the semiconductor wafer 30 through electrical connectors 54 to provide a unitary structure ~~51 as indicated in FIG. 6~~. The unitary structure ~~51~~ is separated along

the scribe lines 32 into a plurality of packages 60, and exemplary one of such packages 60 being shown in FIG. 7. Thus, in this example, each package 60 has a plurality, here four, of the chips 32 with the electrical contacts 53 of the four chips 32 in such package 60 being electrically connected by the spanning electrical conductor 52. A schematic diagram of the package is shown in FIG. 10.--

Please amend the third full paragraph on page 7 beginning at line 16 as follows:

--Next, a plurality of the packages 60 are arranged in a memory module 62 as indicated in FIG. 8. More particularly, here each memory module 62 includes a plurality of, here three, of the packages 60 shown in FIG. 7 and a printed circuit board 66 an electrical interconnects 68 thereon. The memory module 62 is fabricated by mechanically and electrically connecting the ~~four~~ three packages to 60 to the printed circuit board 66. More particularly, the electrical contacts 55 are disposed on and electrically connected to the electrical interconnects 68.--